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OFGS File: IR-1986 DIV (2-2500)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:

Thomas HERMAN

Date: November 28, 2000

Serial No.: Unassigned

Filed: Herewith

For: LOW VOLTAGE MOSFET AND PROCESS FOR ITS MANUFACTURE AND
CIRCUIT APPLICATION

Assistant Commissioner of Patents and Trademarks

Box Patent Application

Washington, DC 20231

REQUEST FOR CONTINUING APPLICATION UNDER 37 C.F.R. 1.53(b)

Sir:

This is a request for the filing of a Division application under the provisions of 37 C.F.R. 1.53(b) of pending application Serial No. 09/436,302, filed November 8, 1999, by Thomas HERMAN entitled LOW VOLTAGE MOSFET AND PROCESS FOR ITS MANUFACTURE AND CIRCUIT APPLICATION. The prior application is hereby incorporated by reference.

Enclosed is a copy of the prior application, including the oath or declaration as originally filed.

I hereby state that the attached papers are a copy of prior application Serial No. 09/436,302, filed November 8, 1999, without any new matter therein.

Cancel in this application original claims 1-8 and 15-19 of the prior application before calculating the filing fee.

The filing fee is calculated as follows:

BASIC Filing Fee: \$ 710.00
Number of Claims in Excess of 20: ____ x \$ 18
Number of Independent Claims over 3: ____ x \$ 80
One or more multiple dependent claims: \$260
TOTAL FILING FEE: \$ 710.00

If checked, Small Entity status is claimed.

Check No. 002301 which includes the amount of \$710.00 in payment of the filing fee is enclosed herewith.

The Patent and Trademark Office is hereby authorized to charge any additional fees or credit any refund, at any time during the prosecution of this application, to Deposit Account No. 15-0700.

Amend the specification by inserting at page 1, line 4, the paragraph:
--This is a division of application Serial No. 09/436,302, filed November 8, 1999.--

This application includes Five (5) sheets of drawings containing figures 1 through 12.

The prior application was assigned to International Rectifier Corporation and is recorded at Reel 010386, Frame 0509.

The power of attorney in the prior application, as originally filed, is to customer no. 2352, OSTROLENK, FABER, GERB & SOFFEN, LLP, 1180 Avenue of the Americas, New York, New York 10036-8403, and the members of the firm: Reg. No. 17,542; Samuel H. Weiner, Reg. No. 18,510; Jerome M. Berliner, Reg. No. 18,653; Robert C. Faber, Reg. No. 24,322; Edward A. Meilman, Reg. No. 24,735; Stanley H. Lieberstein, Reg. No. 22,400; Steven I. Weisburd, Reg. No. 27,409; Max Moskowitz, Reg. No. 30,576; Stephen A. Soffen, Reg. No. 31,063; James A. Finder, Reg. No. 30,173; William O. Gray, III, Reg. No. 30,944; Louis C.

Dujmich, Reg. No. 30,625, and Douglas A. Miro, Reg. No. 31,643, as attorneys with full power of substitution and revocation to prosecute this application, to transact all business in the Patent and Trademark Office in connection therewith and to receive all correspondence. The Power appears in the original papers in the prior application.

SEND CORRESPONDENCE TO: DIRECT TELEPHONE CALLS TO:

OSTROLENK, FABER, GERB & SOFFEN, LLP
1180 Avenue of the Americas
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EXPRESS MAIL CERTIFICATE

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Dorothy Jenkins

Name of Person Mailing Correspondence

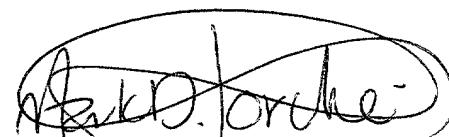
Dorothy Jenkins
Signature

November 28, 2000

Date of Signature

SHW:MDT:ck
Enclosures

Respectfully submitted,



Mark D. Torché
Registration No.: 45,823
OSTROLENK, FABER, GERB & SOFFEN, LLP
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APPLICATION INFORMATION

Title Line One:: LOW VOLTAGE MOSFET AND PROCESS FOR ITS M
Title Line Two:: ANUFACTURE AND CIRCUIT APPLICATION
Total Drawing Sheets:: 5
Formal Drawings?:: Yes
Application Type:: Utility
Docket Number:: 2-2500
Secrecy Order in Parent Appl.?:: No

CONTINUITY INFORMATION

This application is a:: DIVISION OF
> Application One:: 09/436,302
Filing Date:: 11-08-1999

Which is a:: NON PROV. OF PROVISIONAL
>> Application Two:: 60/107,700
Filing Date:: 11-09-1998

Source:: PrintEFS Version 1.0.1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:

Thomas HERMAN

Date: November 28, 2000

Serial No.: Unassigned

Filed: Herewith

For: LOW VOLTAGE MOSFET AND PROCESS FOR ITS MANUFACTURE AND
CIRCUIT APPLICATION

Assistant Commissioner for Patents

Box Patent Application

Washington, D.C. 20231

**PRELIMINARY AMENDMENT TO ACCOMPANYING
DIVISIONAL APPLICATION UNDER 37 C.F.R. §1.53(b)**

Sir:

Preliminary to the examination of the above-identified continuation application being filed herewith, please make the following a part of the record:

IN THE TITLE:

Please amend the title to read as follows:

--PROCESS FOR MANUFACTURING A LOW VOLTAGE MOSFET POWER
DEVICE HAVING A MINIMUM FIGURE OF MERIT--.

IN THE SPECIFICATION:

Amend the specification by inserting at page 1, line 4, the paragraph:

--This is a division of application Serial No. 09/436,302, filed November 18, 1999--.

IN THE CLAIMS:

Cancel claims 1-8 and 15-19.

REMARKS

By this Preliminary Amendment, Applicant has canceled claims 1-8 and 15-19 without prejudice. Accordingly, claims 9-14 are pending in the subject application. Applicant maintains that the above amendments raise no issue of new matter.

In view of the foregoing considerations, it is respectfully submitted that this application is now in condition to be allowed and the early issuance of a Notice of Allowance is respectfully solicited.

EXPRESS MAIL CERTIFICATE

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Dorothy Jenkins

Name of Person Mailing Correspondence

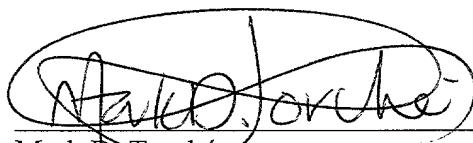
Signature

November 28, 2000

Date of Signature

SHW:MDT:ck

Respectfully submitted,



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- 1 -

LOW VOLTAGE MOSFET AND PROCESS FOR
ITS MANUFACTURE AND CIRCUIT APPLICATION

RELATED APPLICATIONS

5 This application claims the benefit of U.S. Provisional Application No. 60/107,700, filed November 9, 1998.

10 This application is related to application Serial No. 08/946,984 filed October 8, 1997 entitled PROCESS FOR MANUFACTURE OF P CHANNEL MOSGATED DEVICE WITH BASE IMPLANT THROUGH CONTACT WINDOW (IR-1212); application Serial No. 08/956,062 filed October 22, 1997 entitled ZERO ALIGNMENT CELL PROCESS (20 MILLION/IN2) (GEN VI) (IR-1232); U.S. Patent No. 5,795,793 issued August 18, 1998 entitled NEW REDUCED MASK COUNT PROCESS (GEN 6-N CHANNEL) (IR-1113); application Serial No. 09/038,453 filed March 11, 1998 entitled MOS FETs FOR VERY LOW VOLTAGE D-C TO D-C CONVERTERS (IR-1455); all of which are owned by the assignee of the present application.

BACKGROUND OF THE INVENTION

This invention relates to MOSgated power devices and more specifically relates to a novel MOSgated device having a minimum figure of

merit, a novel process for its manufacture, and a novel circuit application of the device.

Low voltage power MOSgated devices, particularly power MOSFETs, are well known and are commonly made with planar or trench topologies. The trench topologies have been used for very low voltage devices which are to have the lowest possible switching losses in high frequency applications such as in d-c to d-c converters used for producing a regulated d-c voltage for portable electronic devices powered from a battery. By reducing switching loss, battery life can be extended for such portables as lap top computers.

Switching loss is determined, in part, by the figure of merit of the MOSFET, which is the product of its on-resistance R_{DSON} and its gate charge Q_g . A minimum figure of merit is desired for high frequency, low voltage MOSFETs. Trench devices have been useful in these applications because it was believed that they had an inherently lower Q_g than that of planar designs.

Planar technology MOSFETs using spaced closed polygonal cells are well known, and are shown, for example, in patent 5,008,725, and in Figure 12 herein. These devices have a relative lower on-resistance R_{DSON} than equivalent trench designs, but, because of the geometry of the polygonal design (usually hexagonal or rectangular base cells) the polysilicon gate extends across areas such as areas 30, shown in Figure 12 for a hexagonal cell topology, which do not contribute to invertible channel width. More

specifically, Figure 12 shows polysilicon web 31 containing windows 32, 33, 34 and 35 used to define diffused bases or channels, shown in dotted lines.

The window openings such as opening 36 was conventionally 5.8 microns in low voltage designs. The polysilicon 31 overlies areas 30, which are inactive, contribute heavily to the polysilicon gate to-drain capacitance, and thus to Q_g .

5 Planar designs have also used a stripe topology, using elongated, spaced base stripes. While these designs have a lower Q_{GD} than cellular designs, they usually have an increased on-resistance, and the figure of merit was not believed to be reduced by the planar stripe design.

10 It would be desirable to use a planar stripe topology for a low voltage power MOSgated device in which the figure of merit, that is, the product of Q_g and $R_{DS(ON)}$ can be reduced.

BRIEF SUMMARY OF THE INVENTION

15 In accordance with the invention, it has been found that a topology, employing parallel base stripes with a polysilicon line spacing between less than about 1.5 microns to about 2.5 microns, with a polysilicon line width of about 2.6 to about 8.0 microns, depending on the drain to source voltage rating. For a 30 volt device, it would be from 3.2 to 3.5 microns, preferably 3.4 microns. A base to base spacing of about 0.8 microns or greater 20 will produce a minimum figure of merit. It has been found that the increased channel width per unit area produced by the closer spacing of the polysilicon lines reduces $R_{DS(ON)}$ proportionally more than Q_g increases, with a practical

minimum figure of merit being reached at a polyline spacing of about 1.5 microns. The figure of merit obtained with this novel geometry is lower than that obtained with equivalent die areas employing either trench technology or closed polygonal cell technology.

5

Further, the present invention produces a device having both an extremely low $R_{DS(ON)}$ and an extremely high avalanche energy.

10

Another feature of the invention employs the polysilicon stripes to define a mask for the formation of three sequential regions, the first being a base (or channel) diffusion, the second being a source diffusion and the third being a higher concentration base region which underlies the first base and which does not invade the invertible channel formed by the first base and source. The third region is formed by an implant through the polysilicon window and a subsequent anneal.

15

A novel application of the invention is for d-c to d-c converter circuits using a control MOSFET and a synchronous rectifier MOSFET. Both of these MOSFETs are made by the process of the invention and differ only in die area.

BRIEF DESCRIPTION OF THE DRAWINGS

20

Figure 1 is a top view of a die which can contain the structure of the present invention.

Figure 2 is a cross-section of the termination region of the die of Figure 1 in circled area "A" in Figure 1 at a first stage of the manufacture of the device.

5 Figure 3 shows the stripe pattern of the polysilicon gate within the active area portion shown in circle "B" in Figure 1.

Figure 4 is a cross-section of Figure 3 taken across section line 4-4 in Figure 3 after the step of forming the polysilicon gate stripes.

10 Figure 5 shows the termination region of Figure 2 after the deposition of polysilicon to form a termination field plate.

Figure 6 shows the structure of Figure 4 after the diffusion of channel and source regions.

Figure 7 shows the structure of Figure 6 after the implant of high concentration deep base regions.

15 Figure 8 shows the structure of Figure 7 after the formation of source and drain electrodes.

Figure 9 shows the variation of channel width (and thus the reciprocal of on-resistance) as a function of polysilicon line spacing.

Figure 10 shows the gate/drain area, and thus Q_G as a function of polysilicon line spacing.

Figure 11 shows a circuit diagram of a d-c to d-c converter using power MOSFETs made in accordance with the invention.

5

Figure 12 shows the polysilicon layout of a prior art MOSFET with a polygonal cell topology

DETAILED DESCRIPTION OF THE DRAWINGS

Referring first to Figure 1, there is shown a typical die 40 which can be processed in accordance with the invention to produce a MOSgated device, for example, a power MOSFET. While the invention is applicable to all voltage ranges, it is particularly useful for devices having a breakdown voltage less than about 60 volts. Die 40 may have top source contact, a gate pad 41 for connection to its polysilicon gate, and a bottom drain contact, as will be described. A silicon wafer is formed with identical die which are simultaneously processed in a silicon wafer and are separated at the end of the process. The terms die, chip and wafer are frequently interchanged. Die 40 may be as large as about 102 mils by 157 mils which is the largest size which can be mounted in a typical SO8 package. Of course any other package can be used.

The first step of the process used to make the device of the invention is the selection of a suitable wafer 50, shown in Figure 2 which has a

highly conductive N⁻ body 51, which may be 375 microns thick (ground down to about 200 microns at the end of the process) and which has an epitaxially formed junction-receiving substrate 52. For a breakdown voltage of about 30 volts, the layer 52 will have a thickness of about 5 microns and a resistivity of about 0.18 Ω cm, which can be considered to be an N⁻ layer.

A 7500 Å thick field oxide layer 53 is first grown atop layer 52 and, in a first mask step, a window 54 is opened in the field oxide and a P⁺ diffusion 55 is formed around the periphery of and under the gate bonding pad of the chip, which will serve as a field termination ring for the final device.

This diffusion may be carried out with a boron implant at a dose of 1E14 and at an energy of 80kV, followed by a diffusion drive at 1050°C for 2 hours.

This will produce the P⁺ region 55 with a depth of about 1.5 microns.

The field oxide 53 is then selectively etched to open the active area of the die. As next shown in Figures 3 and 4, a gate oxide layer 60 is grown over the surface of the layer 52 to a thickness of about 300 Å. A conductive polysilicon layer 61 is then grown atop oxide layer 60 to a thickness of about 0.75 micron. An oxide layer 200 is also grown or deposited atop the polysilicon layer 61. The polysilicon layer 61, oxide layer 60 and oxide layer 200 are then etched into elongated, parallel stripes as shown in Figure 3.

In accordance with the invention, the width of the polysilicon strips 61 (the polyline width) is from 2.6 to 8.0 microns, preferably, 3.2 to 3.5 microns, and, for a 30 volt devise, is preferably 3.4 microns, while the spacing

between the parallel elongated and straight strips 61 is from 1 to 4 microns, preferably 1.5 microns.

During the etch of polysilicon layer 61, the mask used permits the definition of the termination field plate 70 shown in Figure 5. The field plate 70 has a length of about 15 microns, and is spaced from the adjacent end of EQR ring 72 (partially shown in Figure 5) by a gap of 5 to 8 microns.

Thereafter, and as shown in Figure 6, a suitable photolithography step is carried out using oxide strips 200 and polysilicon stripes 61 to define elongated channel and source diffusions 80 and 81 respectively. More specifically, to form channel region 80, a boron implant is used at a dose of 8.5E13 at 80 kV. This implant is then driven at 1125°C for 90 minutes in nitrogen gas, driving the channel implants 80 to a depth of about 1.25 microns. Significantly, the channels 80 are spaced by a common conduction region which is about 0.8 microns wide or greater as shown in Figure 6.

The N⁺ source regions 81 are then formed using an arsenic implant at a dose of 8E15 at 120 kV. This implant is then driven at 975°C for 90 minutes, driving the source regions to a depth of about 0.4 microns, and forming invertible channel regions 82 within bases 80.

Thereafter, and as shown in Figure 7, and in accordance with a separate feature of the invention, a P⁺ region 85 is implanted through the same windows which defined the channel and source regions 80 and 81 respectively.

To prevent the invasion of channel region 82 by the heavily doped regions 85, the regions are formed by a boron implant at a dose of 2E15 at 150 kV followed by an anneal of 30 minutes at 975°C. The P⁻ regions 85 increase the ruggedness of the device and reduce the R_b of the bases 80.

5 Thereafter, the source aluminum contact 90 (Figure 8) is connected to the source and channel regions by the process described in copending application Serial No. 08/956,062 (IR-1232). Thus, as shown in Figure 8, an insulation layer 95, consisting, for example of a low temperature oxide and having side wall spacers 96 are formed over the polysilicon stripes 10 61 to insulate them from the source contact 90. The layer 95 may have a thickness of about 0.6 to 0.7 microns. An etch operation is then carried out to etch shallow trenches 98 in and through and along the center of each source region 81 and into the underlying channel region 80. The trenches are preferably narrower than the space between side wall spacers to expose a short 15 planar ledge at the silicon surface to improve the contact to the aluminum source layer 90.

The contact 90 may then receive an insulation coating (not shown) and may be patterned to enable the etching and definition of the gate pad 41 and the termination as desired.

20 A bottom metal 99 is then applied to the bottom of the chip to act as the drain contact.

Figures 9 and 10 show the design trade-offs which are employed in the present invention, comparing the stripe topology of the present invention to known cellular topology. Referring to Figure 9, it can be seen that the total channel width of a chip of given area increases as the polyline spacing is decreased. A larger channel width is desired because it reduces the on-resistance of the device. In the prior art hexagonal cell device of Figure 12, a line spacing of 5.8 microns is used for lower voltage devices. As shown in Figure 9, this yields a larger channel width than a stripe geometry with similar spacing. Figure 10 shows the known advantage of the stripe geometry over the cellular in terms of Q_g . The difference in Q_g , however, is minimized at larger polyline spacings.

It has been found that the stripe geometry will produce a larger channel width per unit area for polyline spacings in the region between about 1 to 4 microns, particularly at about 1.5 microns, surprisingly with no increase of $R_{DS(on)}$.

Thus, in accordance with the invention, it has been found that a minimum figure of merit is obtained with a choice of a polyline spacing of from 1 to 4 microns and a polyline width of from 3.2 to 3.4 microns.

Figure 11 shows a circuit diagram employing power MOSFETs made in accordance with the invention. Thus, the circuit of Figures 11 is a d-c to d-c buck converter circuit comprising an input d-c terminal 110, which may be a nominally 14 volt battery connected to the source of a high frequency control MOSFET 111 and in series with an inductor 112 to a d-c output

terminal which can, for example, be at a regulated 1.5 volts. A synchronous rectifier MOSFET 113 is connected from the node between MOSFET 111 and inductor 112 to ground. A suitable control integrated circuit 114 is programmed to produce gate signals to control the turn on and turn off of MOSFETs 111 and 113 in a suitable and known sequence to produce the desired output d-c voltage even though the input d-c voltage fluctuates as due to aging of an input battery, temperature changes, state of charge and the like.

In the past, MOSFET 111 was chosen to have a minimum switching loss while the synchronous rectifier MOSFET was chosen for low conduction loss (that is, low $R_{DS(on)}$). Thus, the MOSFETs had different manufacturing techniques, for example, a trench technology for MOSFET 111 and a planar cellular technology for MOSFET 113.

In accordance with an important feature of this invention, both MOSFETs 111 and 113 can advantageously employ the planar stripe technology shown for the device of Figures 1 and 8, and the die would differ only in size. Thus, MOSFET 111 has lower current requirements than MOSFET 113 and needs a die size, for example, of 56 mil by 140 mil. MOSFET 113 can have a die size of 102 mil by 157 mil; both die separately housed in SO8 style packages or copacked if desired.

Although the present invention has been described in relation to particular embodiments thereof, many other variations and modifications and other uses will become apparent to those skilled in the art. It is preferred,

therefore, that the present invention be limited not by the specific disclosure herein, but only by the appended claims.

WHAT IS CLAIMED IS:

1. A MOSgated semiconductor device having a minimized figure of merit; said device comprising:

 a die of monocrystalline silicon having a body region and an upper junction receiving layer of one conductivity type;

5 a plurality of elongated spaced and parallel base stripe diffusions of the other conductivity type formed in the upper surface of said junction receiving layer and a plurality of elongated source diffusions of the one conductivity type in and extending coextensively with said base stripe diffusions to define invertible channel regions along the sides of each of said elongated base stripe diffusions;

10 a plurality of gate stripes each comprising gate oxide stripes covered by conductive polysilicon stripes; said plurality of gate stripes overlying respective spaced pairs of adjacent invertable channel regions and the space between their respective base diffusions; said polysilicon stripes each having a width in the range of about 3.2 microns to 3.5 microns and a spacing in the range of about 1.0 to 4.0 microns;

15 adjacent ones of said base diffusions being spaced apart by greater then about 0.8 micron.

2. The device of claim 1 wherein said polysilicon stripes have a width of about 3.1 microns and a spacing of about 1.5 microns.

3. The device of claim 1 wherein said base diffusion have a depth of about 1.25 microns and said source diffusions have a depth of about 0.4 microns.

4. The device of claim 2 wherein said base diffusion have a depth of about 1.25 microns and said source diffusions have a depth of about 0.4 microns.

5. The device of claim 1 which further includes a plurality of second base diffusions of the other conductivity type which are centered on respective ones of said base diffusions and which have a higher concentration then that of said base diffusions and which have a lateral extent defined by the spacing of said polysilicon stripes.

6. The device of claim 2 which further includes a plurality of second base diffusions of the other conductivity type which are centered on respective ones of said base diffusions and which have a higher concentration then that of said base diffusions and which have a lateral extent defined by the spacing of said polysilicon stripes.

7. The device of claim 3 which further includes a plurality of second base diffusions of the other conductivity type which are centered on respective ones of said base diffusions and which have a higher concentration then that of said base diffusions and which have a lateral extent defined by the spacing of said polysilicon stripes.

8. A MOSgated semiconductor device having a minimized figure of merit; said device comprising:

a die of monocrystalline silicon having a body region and an upper junction receiving layer of one conductivity type;

5 a plurality of elongated spaced and parallel base stripe diffusions of the other conductivity type formed in the upper surface of said junction receiving layer and a plurality of elongated source diffusions of the one conductivity type in and extending coextensively with said base stripe diffusions to define invertible channel regions along the sides of each of said 10 elongated base stripe diffusions;

a plurality of gate stripes each comprising gate oxide stripes covered by conductive polysilicon stripes; said plurality of gate stripes overlying respective spaced pairs of adjacent invertable channel regions and the space between their respective base diffusions;

15 a plurality of second base diffusions of the other conductivity type which are centered on respective ones of said base diffusions and which have a higher concentration then that of said base diffusions and which have a lateral extent defined by the spacing of said polysilicon stripes.

9. The process of manufacture of a MOSgated device comprising the steps of forming a gate oxide layer atop a silicon surface of one conductivity type; forming a layer of polysilicon atop said gate oxide layer; etching said polysilicon layer and the said underlying gate oxide layer into a 5 plurality of spaced stripes of oxide and polysilicon overlying said oxide; implanting and diffusing a plurality of spaced first base diffusion stripes of the other conductivity type into said silicon surface, using said stripes of

polysilicon as a mask; implanting and diffusing a plurality of source diffusions into said first base diffusion stripes, using said stripes of polysilicon as a mask, and leaving invertible channel regions along the outer edges of said first base diffusion stripes; diffusing third base diffusion stripes, into said silicon surface, using said stripes of polysilicon as a mask, to a depth about equal to that of said first diffusions and a width substantially equal to the space between the opposite edges of adjacent pairs of said polysilicon stripes.

10. The process of claim 9, wherein said polysilicon stripes have a width of about 3.1 microns and a spacing of about 1.25 microns.

11. The process of claim 9 wherein said first base diffusions have a depth of about 0.4 microns and said second base diffusions have a depth of about 1.25 microns.

12. The process of claim 10 wherein said first base diffusions have a depth of about 0.4 microns and said second base diffusions have a depth of about 1.25 microns.

13. The process of claim 9 which further includes the formation of insulation spacer layers over the type and edges of said polysilicon stripes and the etching of shallow openings through central portions of said source regions and into said first base diffusions; and 5 thereafter depositing a metal layer over the upper surface of said device to contact said source regions and said first and second base diffusions.

14. The process of claim 12 which further includes the formation of insulation spacer layers over the type and edges of said polysilicon stripes and the etching of shallow openings through central portions of said source regions and into said first base diffusions; and thereafter depositing a metal layer over the upper surface of said device to contact said source regions and said first and second base diffusions.

15. A d-c to d-c converter circuit which includes a high frequency control MOSFET connected in series with a d-c source, an inductor and a d-c output and a synchronous rectifier MOSFET connected in closed circuit relation with said inductor and said d-c output; each of said control MOSFET and synchronous rectifier MOSFET being made with identical planar parallel stripe topologies but having different die areas; said synchronous rectifier area MOSFET having a die area which is greater than that of said control MOSFET.

16. The circuit of claim 15 wherein said identical topologies for each of said control MOSFET and synchronous rectifier MOSFET comprises, for each die:

5 a die of monocrystalline silicon having a body region and an upper junction receiving layer of one conductivity type; a plurality of elongated spaced and parallel base stripe diffusions of the other conductivity type formed in the upper surface of said junction receiving layer and a plurality of elongated source diffusions of the one conductivity in and extending coextensively with said base stripe diffusions to

10 define invertible channel regions along the sides of each of said elongated base stripe diffusions;

15 a plurality of gate stripes each comprising gate oxide stripes covered by conductive polysilicon stripes; said plurality of gate stripes overlying respective spaced pairs of adjacent invertable channel regions and the space between their respective base diffusions; said polysilicon stripes each having a width in the range of about 3.2 microns to 3.5 microns and a spacing in the range of about 1.0 to 4.0 microns;

adjacent ones of said base diffusions being spaced apart by greater then about 0.8 micron.

17. The circuit of claim 16, wherein said polysilicon stripes have a width of about 3.1 microns and a spacing of about 1.5 microns.

18. The circuit of claim 17, wherein said base diffusion have a depth of about 1.25 microns and said source diffusions have a depth of about 0.4 microns.

19. The circuit of claim 16 which further includes a plurality second base diffusions of the other conductivity type which are centered on respective ones of said base diffusions and which have a higher concentration then that of said base diffusions and a depth which is greater than that of said base diffusions and which has a lateral extent defined by the spacing of said polysilicon stripes.

LOW VOLTAGE MOSFET AND PROCESS FOR
ITS MANUFACTURE AND CIRCUIT APPLICATION

A power MOSFET die with a minimized figure of merit has of a planar stripe MOSFET geometry in which parallel diffused bases (or channels) are formed by implantation and diffusion of impurities through parallel elongated and spaced polysilicon stripes wherein the polysilicon line width is from about 3.2 to 3.4 microns, preferably 3.4 microns; the polyline spacing is from about 1 to 4 microns, preferably 1.5 microns and the diffused bases are spaced by greater than about 0.8 microns. The polysilicon stripes act as masks to the sequential formation of first base stripes, the source stripes and second higher concentration base stripes which are deeper than the first base stripes. Insulation side wall spacers are used to define a contact etch for the source contact. The above design geometry is used for both the forward control MOSFET and the synchronous rectifier MOSFET of a buck converter circuit.

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(2-1751)

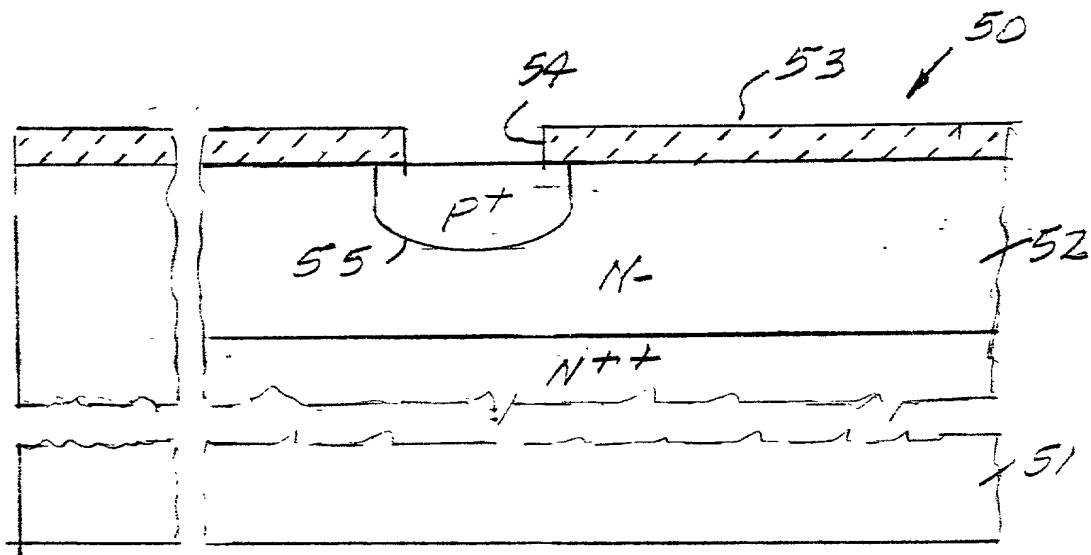
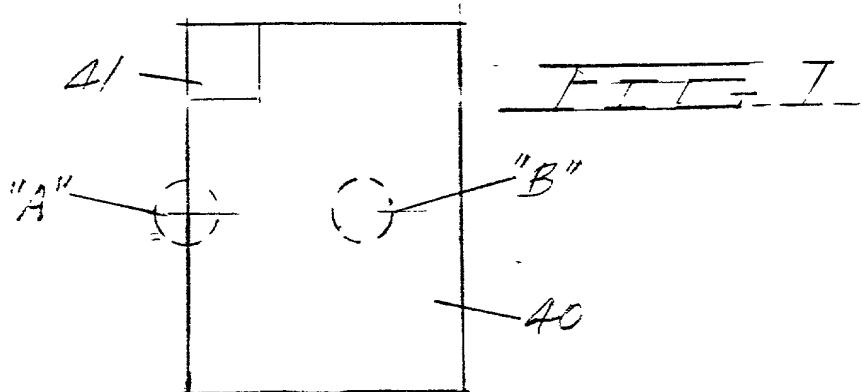


FIG. 2.

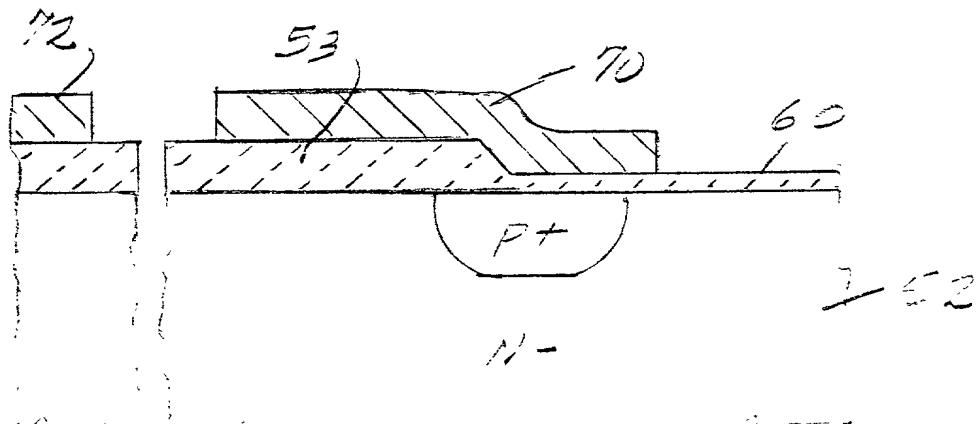
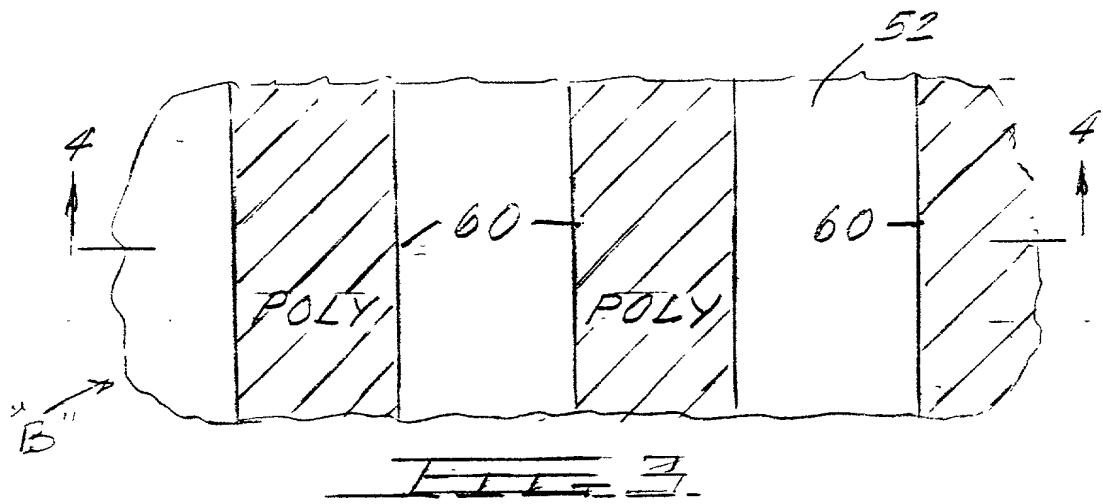
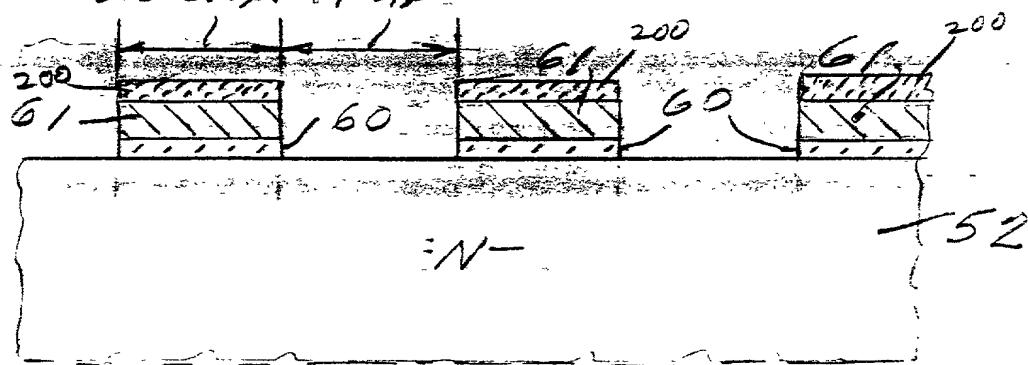
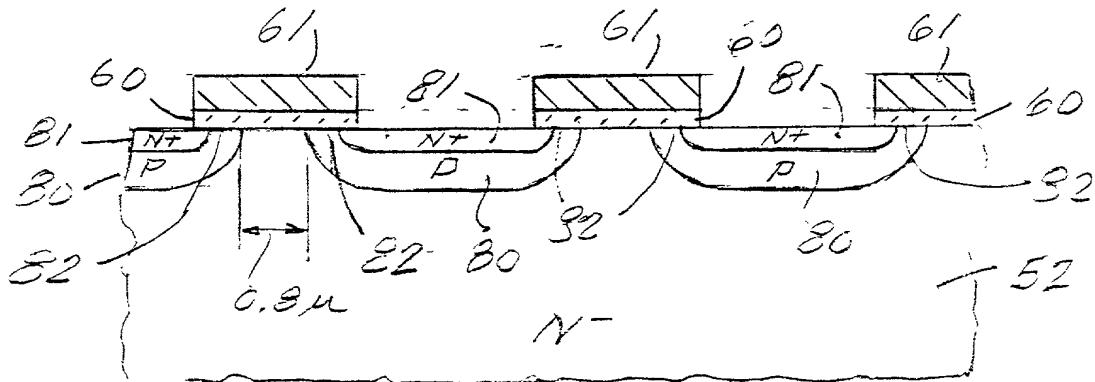


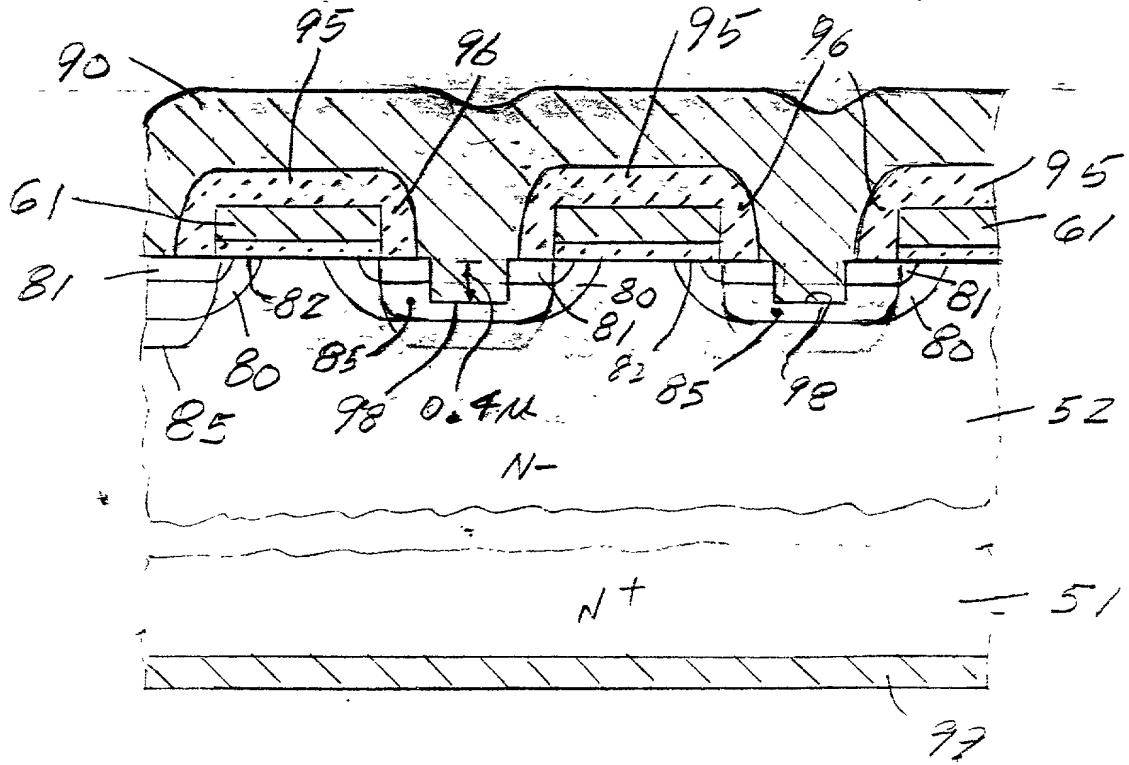
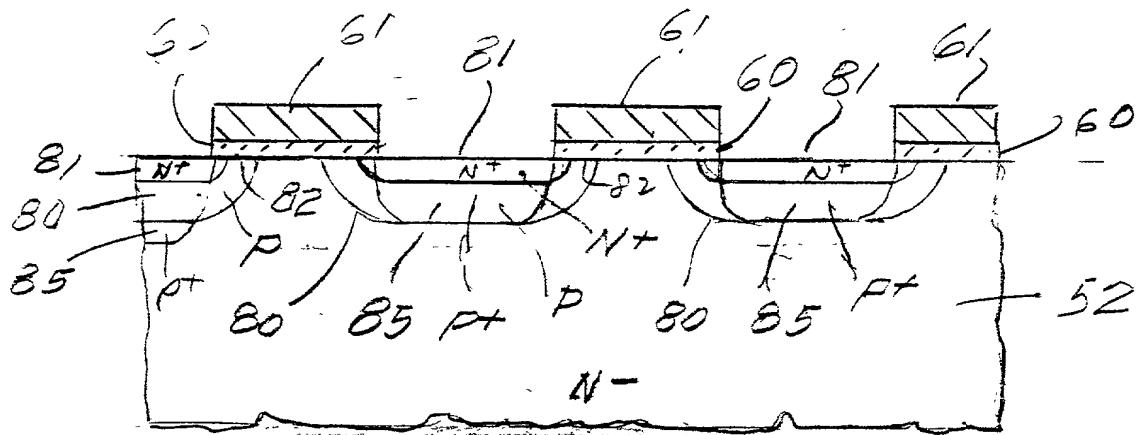
FIG. 5.



3.2-3.5μ 11-44

FIG. 4.FIG. 5.

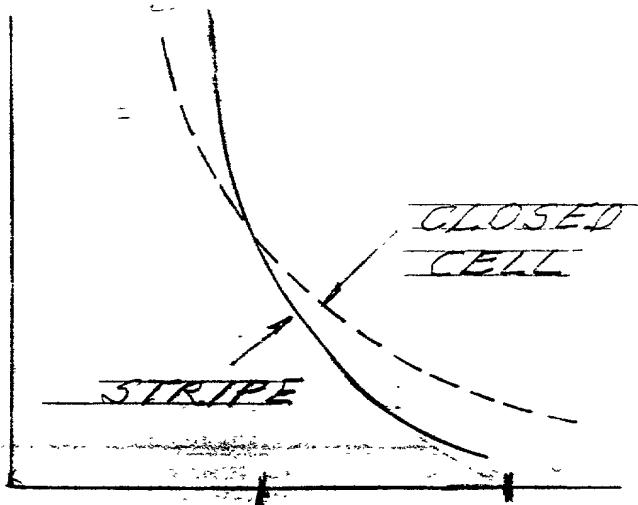
HTT-7



THE B

FIG. 9.

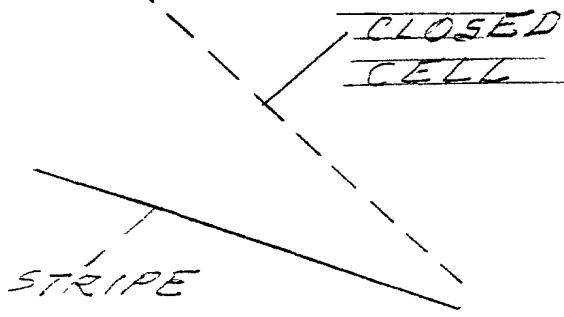
CHANNEL
WIDTH
(WROSON)



1.5μ 5.8μ
POLYLINE SPACING
(FOR 3.4μ POLYLINE WIDTH)

FIG. 11.

Q_g



1.5μ 5.3μ
POLYLINE SPACING
(FOR 3.4μ POLYLINE WIDTH)

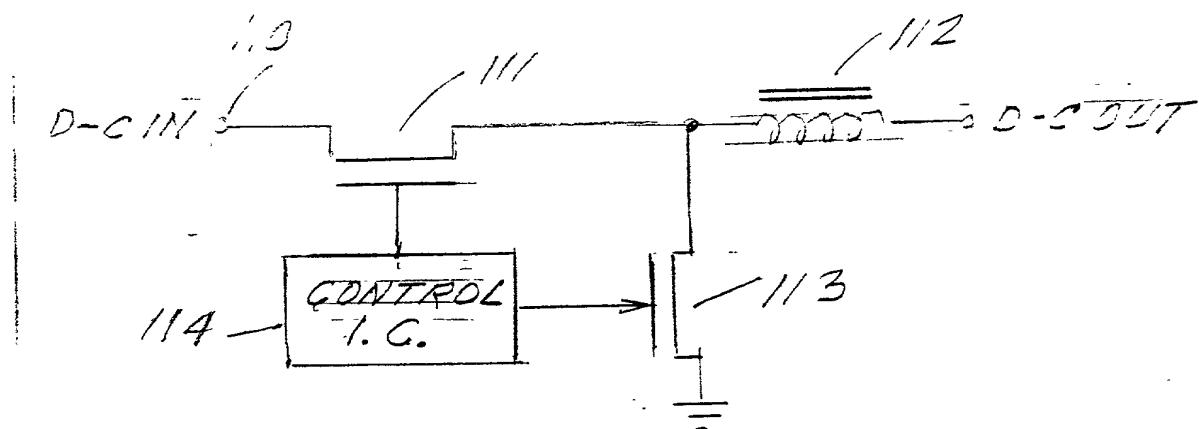


FIG. 77

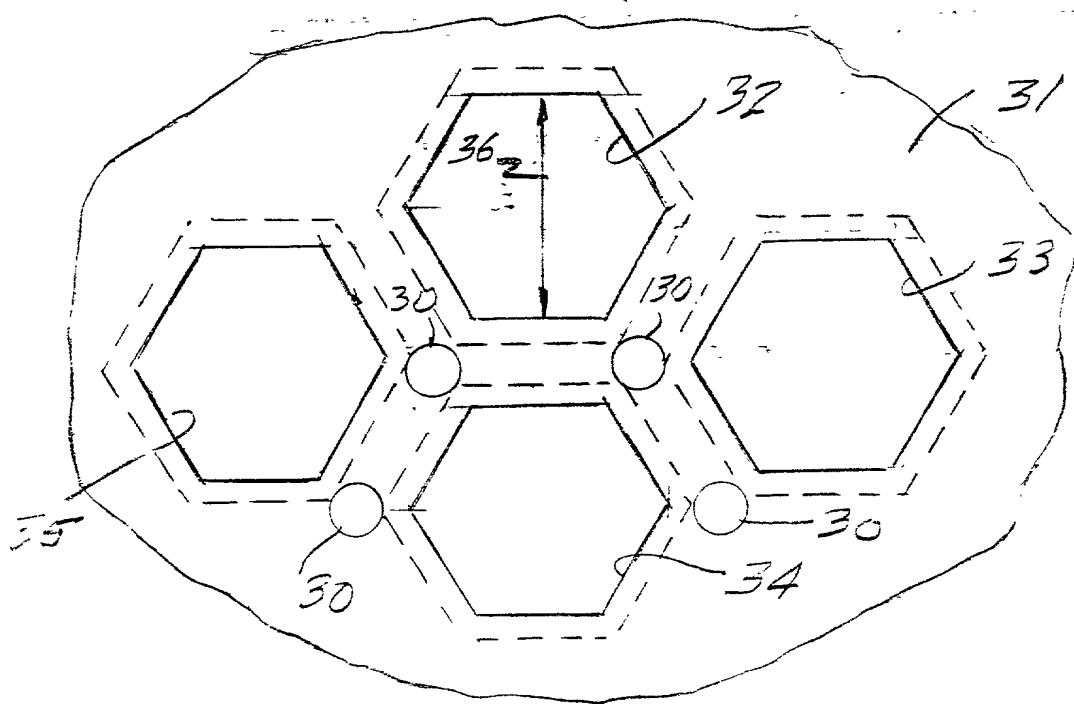


FIG. 78

19-7531
(2-1751)

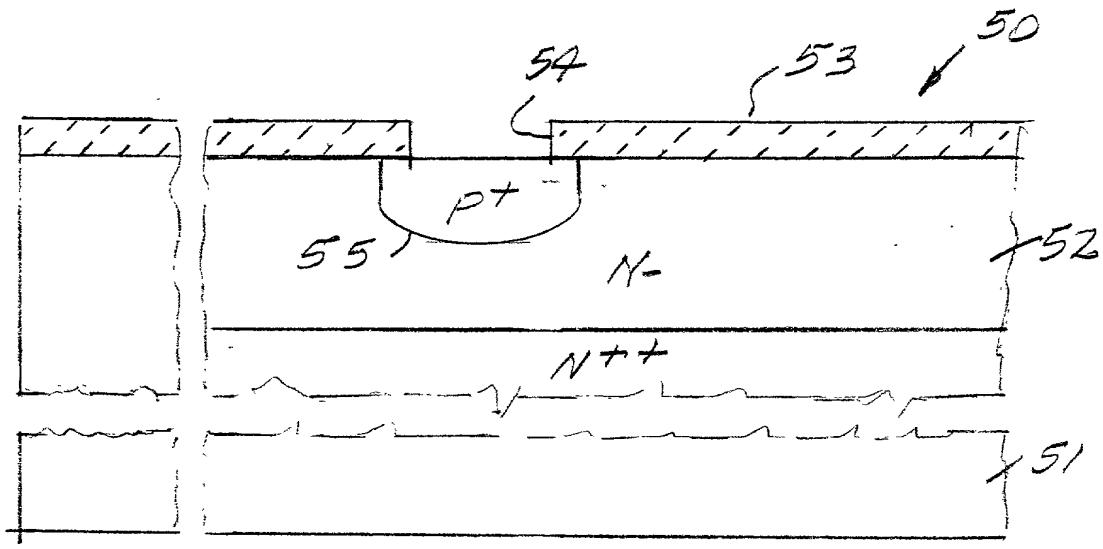
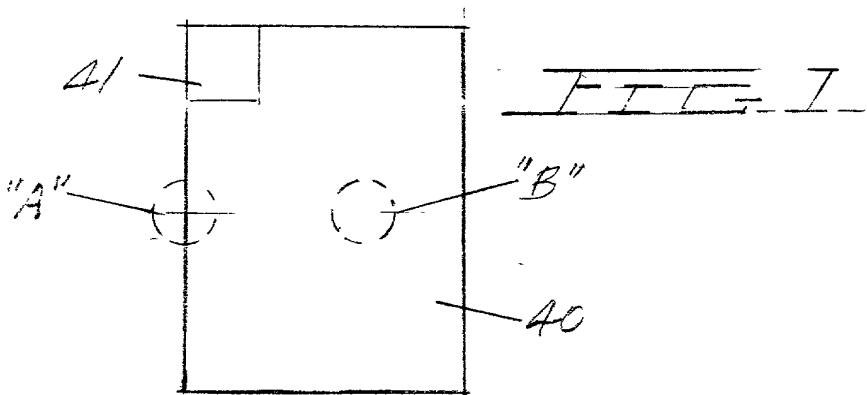


FIG. 2.

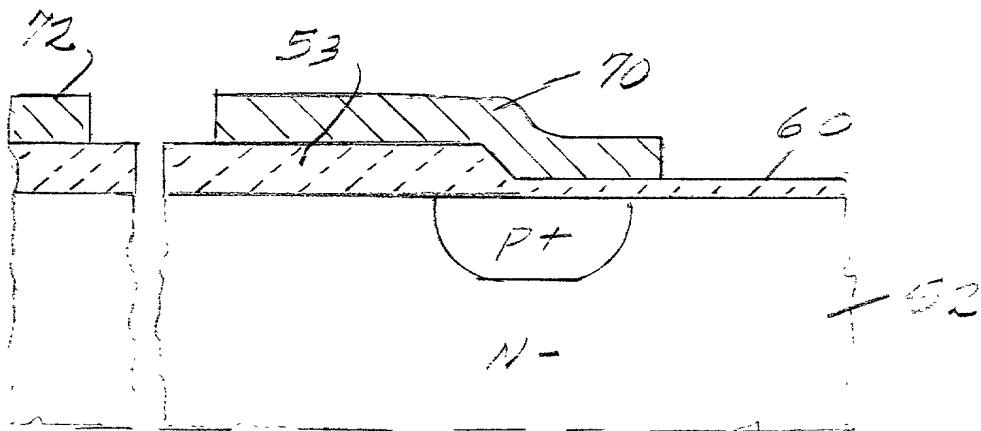
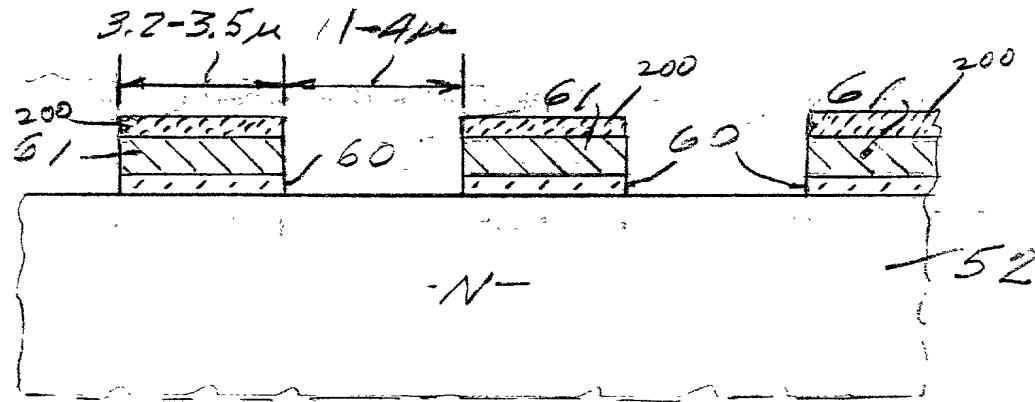
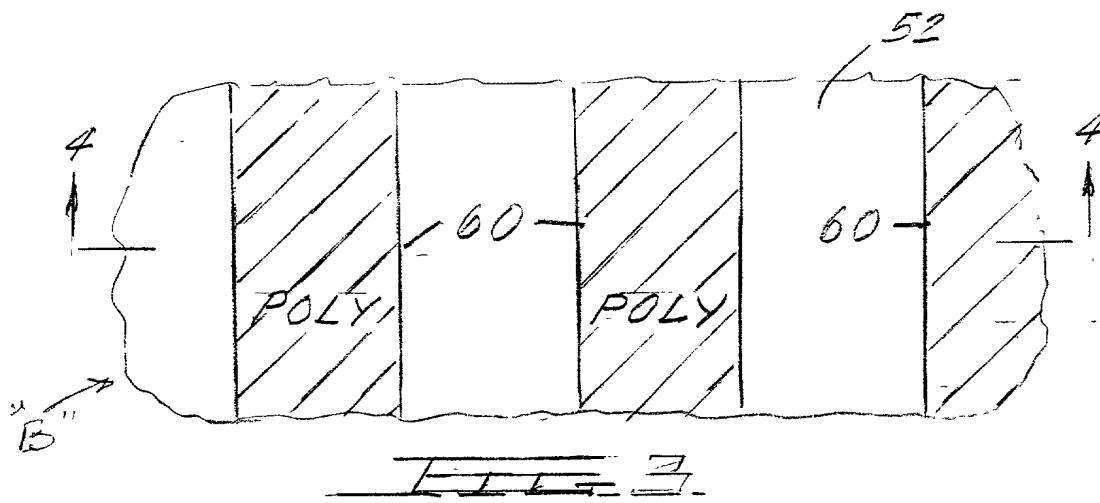
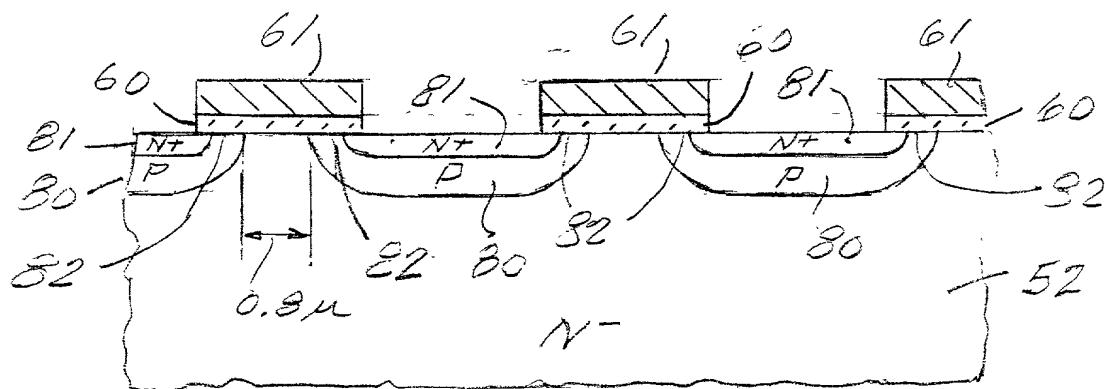


FIG. 3.



TIT-4



TIT-5

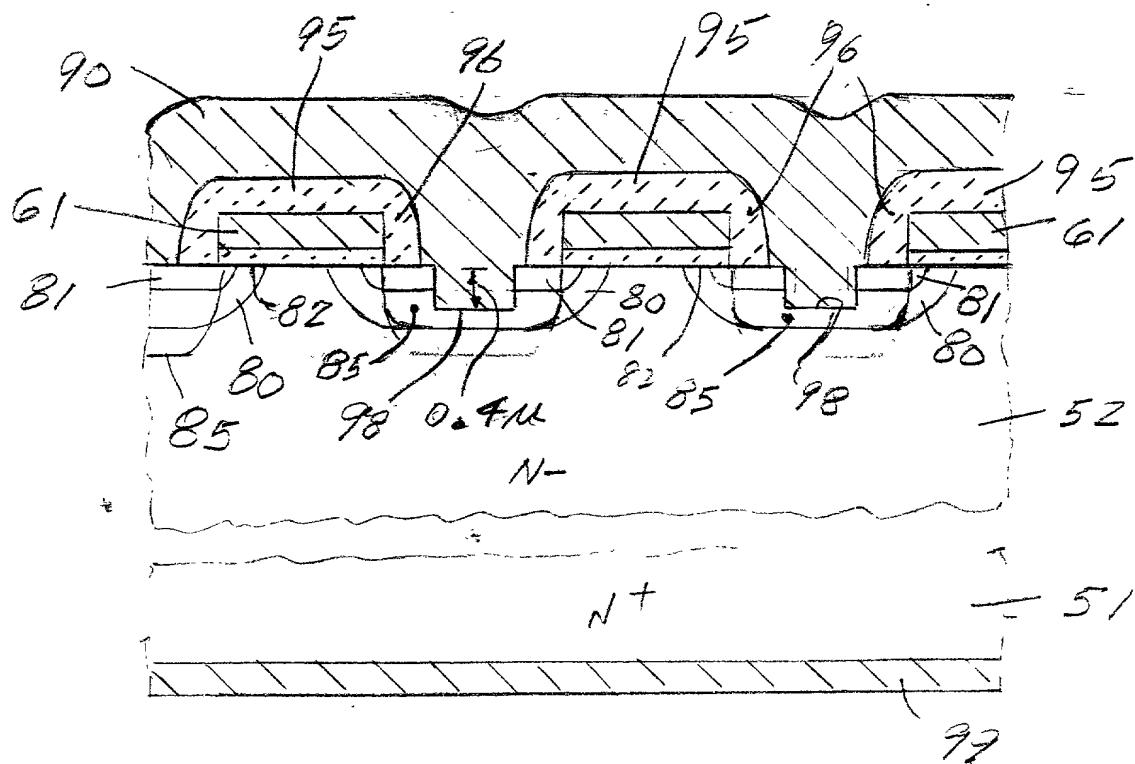
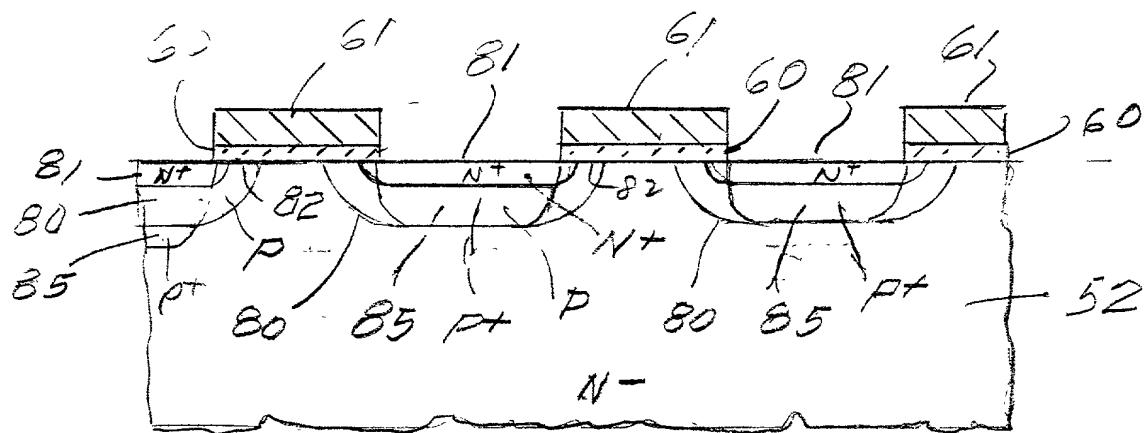
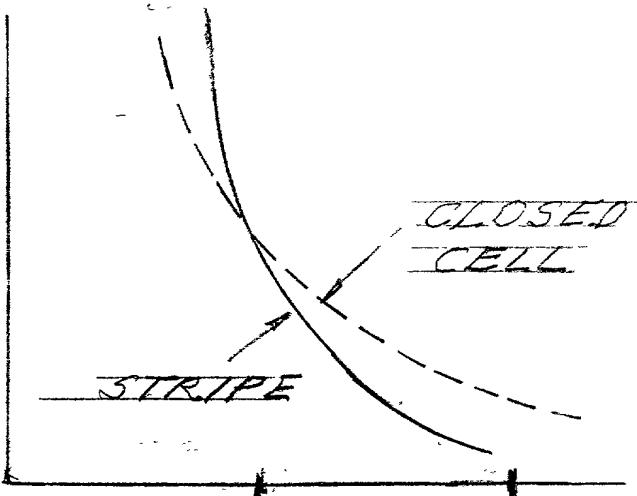
FIG. 7FIG. 8

FIG. 9.

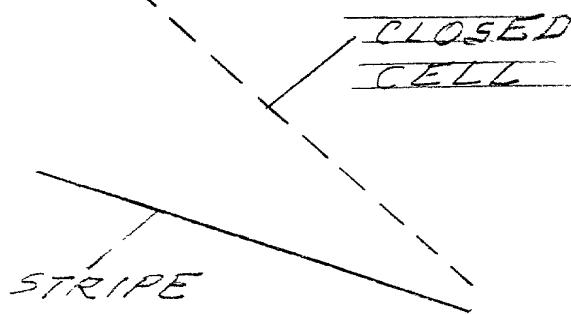
CHANNEL
WIDTH
(WROSON)



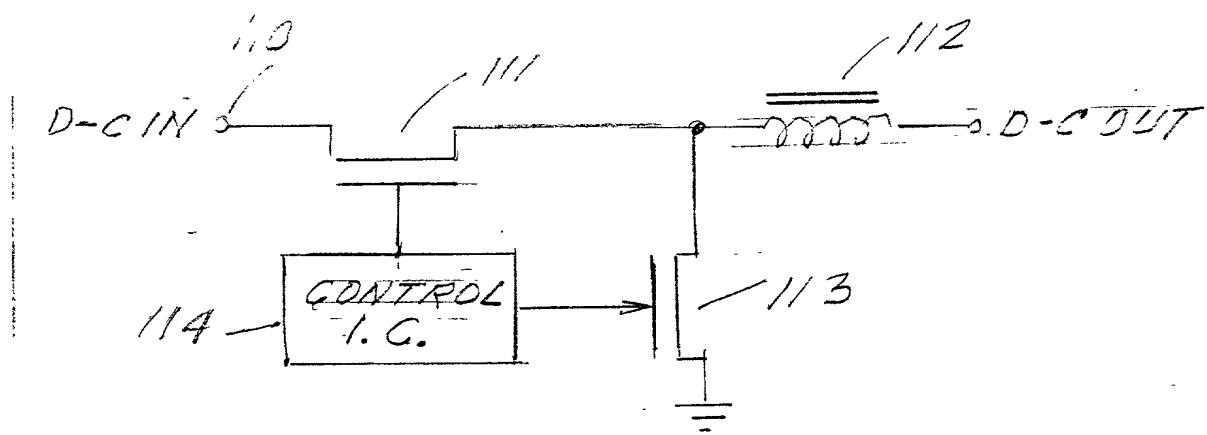
1.5 μ 5.3 μ
POLYLINE SPACING
(FOR 3.4 μ POLYLINE WIDTH)

FIG. III.

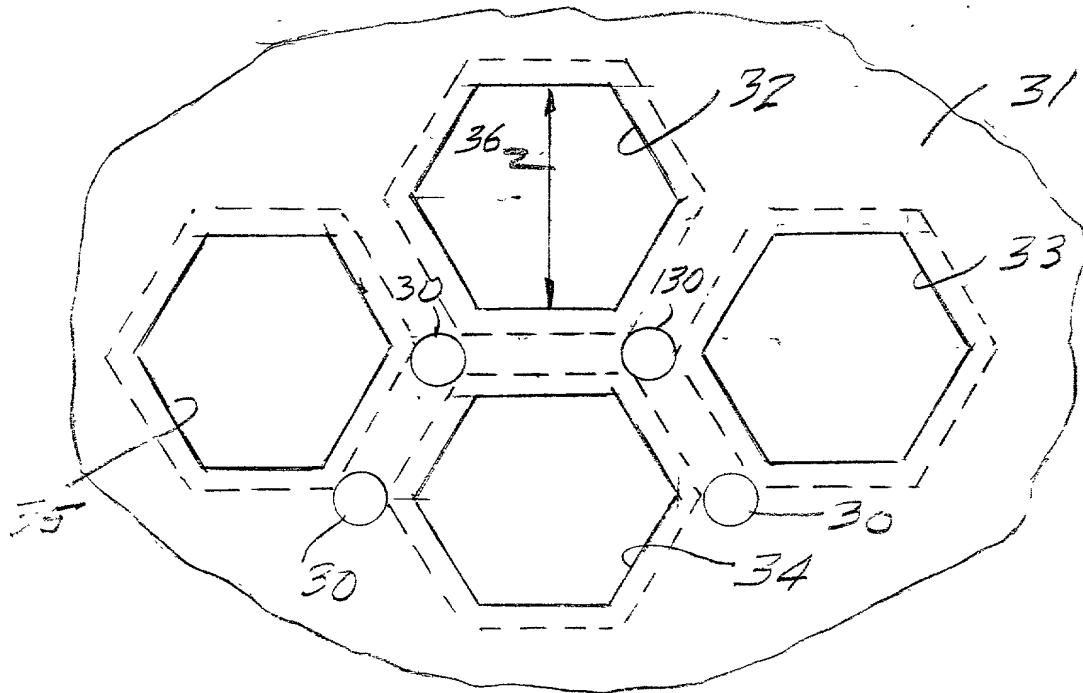
Q_g



1.5 μ 5.3 μ
POLYLINE SPACING
(FOR 3.4 μ POLYLINE WIDTH)



~~FIG. 11~~



~~FIG. 12~~

UNITED STATES OF AMERICA
COMBINED DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATIONOFGS FILE NO.
IR-1531 (2-)

As a below named inventor, I hereby declare that my residence, post office address and citizenship are as stated below next to my name, that I verify believe that I am the original, first and sole inventor (if only one name is listed below) or a joint inventor (if plural inventors are named) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

LOW VOTAGE MOSFET AND PROCESS FOR ITS MANUFACTURE AND CIRCUIT
APPLICATION

the specification of which is attached hereto, unless the following box is checked:

was filed on _____ as United States patent Application Number or PCT International patent application number _____ and was amended on _____ (if any)

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose all information known to be material to patentability in accordance with Title 37, Code of Federal Regulations, §1.56.

I hereby claim priority benefits under Title 35, United States Code §119 of any foreign application(s) for patent or inventor's certificate or United States provisional application(s) listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign or Provisional Application(s)

| COUNTRY | APPLICATION NUMBER | DATE OF FILING (day, month, year) | PRIORITY CLAIMED UNDER 35 U.S.C. 119 |
|---------------|--------------------|--------------------------------------|--|
| United States | 60/107,700 | November 9, 1998 | YES <input checked="" type="checkbox"/> NO _____ |
| | | | YES _____ NO _____ |
| | | | YES _____ NO _____ |

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, §1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application.

| UNITED STATES APPLICATION NUMBER | DATE OF FILING (day, month, year) | STATUS (patented, pending, abandoned) |
|-------------------------------------|--------------------------------------|--|
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I hereby appoint customer no. 2352 OSTROLENK, FABER, GERB & SOFFEN, LLP, and the members of the firm, Samuel H. Weiner - Reg. No. 18,510; Jerome M. Berliner - Reg. No. 18,653; Robert C. Faber - Reg. No. 24,322; Edward A. Meilman - Reg. No. 24,735; Stanley H. Lieberstein - Reg. No. 22,400; Steven I. Weisbord - Reg. No. 27,409; Max Moakowitz - Reg. No. 30,576; Stephen A. Soffen - Reg. No. 31,063; James A. Funder - Reg. No. 30,173; William O. Gray, III - Reg. No. 30,944; Louis C. Dujmich - Reg. No. 30,625 and Douglas A. Miro - Reg. No. 31,643, as attorneys with full power of substitution and revocation to prosecute this application, to transact all business in the Patent & Trademark Office connected therewith and to receive all correspondence.

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NEW YORK, NEW YORK 10036-8403
CUSTOMER NO. 2352

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| | | |
|---|---------------------------------------|----------------------|
| FULL NAME OF SOLE OR FIRST INVENTOR Thomas Herman | INVENTOR'S SIGNATURE Thomas Herman | DATE Nov. 5, 1999 |
| RESIDENCE (City and either State or Foreign Country) Manhattan Beach, California 90266 | COUNTRY OF CITIZENSHIP U.S.A. | |
| POST OFFICE ADDRESS 3113 Palm Avenue, Manhattan Beach, California 90266 | | |